

PATENT ABSTRACTS OF JAPAN

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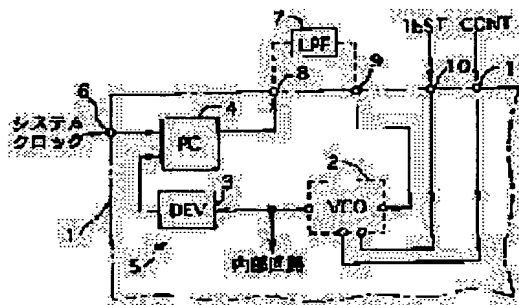
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(54) PLL CIRCUIT

(57)Abstract:

PROBLEM TO BE SOLVED: To test a PLL circuit under a test environment for a digital integrated circuit.

SOLUTION: The circuit is provided with a 1st switch element inserted into a feedback path of a VCO 2 of the PLL circuit 5, a 2nd switch element inserted between the feedback path and a test signal input terminal, and a control means controlling complementarily on/off of the 1st and 2nd switch elements. When the 1st switch element is open, the 2nd switch element is closed, the feedback path of the VCO 2 is interrupted and the oscillation is stopped and an optional test signal is given to the VCO 2 via the 2nd switch element. Thus, the optional test signal is generated by a logic tester and an output of a PC 4 is monitored by the tester to conduct digitally the operating test including at least part of the VCO 2, a DEV 3 and the PC 4.



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CLAIMS

[Claim(s)]

[Claim 1] A voltage-controlled oscillator which outputs a signal of frequency according to control voltage A counting-down circuit which carries out dividing of the output of this voltage-controlled oscillator A phase comparator which detects phase contrast of an output of this counting-down circuit, and a reference signal, and a low pass filter which changes an output of this phase comparator into said control voltage It is the PLL circuit equipped with the above, and is characterized by having the 1st switch element inserted in the feedback loop of said voltage-controlled oscillator, the 2nd switch element inserted between this feedback loop and a test signal input terminal, and a control means which answers logic of a control signal input terminal and controls turning on and off of said 1st and 2nd switch elements complementary.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[The technical field to which invention belongs] Especially this invention relates to the PLL circuit carried in a digital IC about a PLL circuit.

[0002]

[Description of the Prior Art] Although high-frequency-ization of the clock signal accompanying the improvement in a working speed of a digital IC has caused the problem of the electric wave noise radiation to the device exterior not a little by one side, the clock signal generating circuit using PLL (Phase Locked Loop) is effective in the measure for this problem.

[0003] It is because PLL detects the phase contrast of the dividing output and reference signal with a phase comparator (PC), changes the phase contrast signal into direct current voltage with a low pass filter (LPF), and considers [dividing of the output of a voltage-controlled oscillator (VCO) is carried out with a counting-down circuit (DEV),] as the control voltage of VCO further and VCO and a part of DEV serve as a RF portion, as shown in drawing 5 .

[0004]

[Problem(s) to be Solved by the Invention] However, if it was in this conventional PLL circuit, especially, actuation of a phase comparator (PC) and a low pass filter (LPF) is analog-like, and there was a trouble of not getting used to the test atmosphere of a digital IC. Then, let this invention be the enabling-it [to fully examine also by the test atmosphere of a digital IC] purpose.

[0005]

[Means for Solving the Problem] A voltage-controlled oscillator which outputs a signal of frequency according to control voltage in order that this invention may attain the above-mentioned purpose (VCO), A counting-down circuit which carries out dividing of the output of this voltage-controlled oscillator (VCO) (DEV), In a PLL circuit which has a phase comparator (PC) which detects phase contrast of an output of this counting-down circuit (DEV), and a reference signal, and a low pass filter (LPF) which changes an output of this phase comparator (PC) into said control voltage The 1st switch element inserted in the feedback loop of said VCO, and the 2nd switch element inserted between this feedback loop and a test signal input terminal, It is characterized by having a control means which answers logic of a control signal input terminal and controls turning on and off of said 1st and 2nd switch elements complementary.

[0006] If the 1st switch element is turned off, while according to this the 2nd switch element will be in an ON state, the feedback loop of VCO will be cut and oscillation actuation will stop, a test signal of

arbitration is inputted into VCO through the 2nd switch element. Therefore, while generating a test signal of arbitration in a logic circuit tester, it becomes possible by carrying out the monitor of the output of PC by this circuit tester to perform a performance test which contains PC in a part and a DEV list of VCO at least under the test atmosphere of a digital IC.

[0007]

[Embodiment of the Invention] Hereafter, the example of this invention is explained based on a drawing. Drawing 1 · drawing 3 are drawings showing one example of the PLL circuit concerning this invention. First, a configuration is explained. In drawing 1, the PLL circuit 5 containing the voltage-controlled oscillator 2 (following, VCO), a counting-down circuit 3 (following, DEV), and a phase comparator 4 (the following, PC) is built in this digital IC 1, and 1 is a digital IC and it supplies [this PLL circuit 5 generates the clock signal of the frequency which carried out the system clock supplied to a terminal 6 n times (n is the division ratio of DEV3), and] an internal circuitry. In addition, a terminal to carry out external [of the low pass filter 7 (following, LPF) which is one of the components of PLL] to the terminals 8 and 9 of dedication, and for 10 input a test signal (following, TEST), and 11 are the terminals for inputting a control signal (following, CONT).

[0008] 2d of oscillation sections which contain feedback loop 2c in delay circuit 2a and a phase inversion element 2b list as VCO2 shows the configuration to drawing 2, 2h of 2nd switch element inserted between 1st switch element 2e inserted in feedback loop 2c, node 2f of the input side of delay circuit 2a, and 2g of test signal input terminals, It ****, and the 1st and 2nd switch elements 2e and 2h answer the logic of control signal input terminal 2i, are turned on and off complementary (another side is off when one side turns on), and serve as the control means of a publication to the summary of invention.

[0009] When the control voltage from LPF7 is a predetermined value, the time delay of delay circuit 2a is set up so that it may become the time amount which is equivalent to 1/2 period (180 degrees of phase contrast) of oscillation frequency about, and has secured the 360-degree phase change required for an oscillation together with the phase contrast of phase inversion element 2b. Incidentally, the thing of a configuration of being shown in drawing 3 can be used for delay circuit 2a. In drawing 3, some (in drawing, they are two pieces, 22 and 24) power supplies of the odd inverters 22-26 connected to multistage between the terminal 20 and the terminal 21 It is supplied through the constant current source 27 and the variable-resistance element 28, and increase and decrease of the resistance (channel on resistance value of the nMOS transistors 28a-28c) of the variable-resistance element 28 of change are carried out according to the control voltage from LPF7. The time difference which is equivalent to a part for threshold change between logic change of a terminal 20 and logic change of a terminal 21 is produced by shaking the threshold of inverters 22 and 24 up and down.

[0010] In the above configuration, by the logic circuit tester which set the digital IC 1, while generating a system clock, a test signal (TEST), and a control signal (CONT), these signals are impressed to the terminal 6, the terminal 10, and terminal 11 of a digital IC 1, respectively, and if the monitor of the signal which appeared in the terminal 8 is carried out with a logic circuit tester, the performance test which contains PC4 in the part and DEV3 list of VCO2 can be performed in digital one at least. Therefore, other trials of a digital IC 1 and environmental communalization can be attained, and the advantageous effect which is not in the conventional technology in which trial effectiveness is improvable is acquired.

[0011] In addition, drawing 4 is other examples of VCO. This example connects resistance 31, the phase inversion element 32, and the capacity 33 and 34 of pi mold to a quartz resonator 30 and juxtaposition,

and constitutes the feedback loop 35. Furthermore, the variable-capacity device (for example, varicap) 36 from which capacity value is changed to one capacity 33 and juxtaposition according to the control voltage from LPF7 The 1st switch element 38 which it had the configuration of connecting through the capacity 37 for DC blocking, and also was inserted in feedback loop 35a between the end of a quartz resonator 30, and the input of the phase inversion element 32, It has the 2nd switch element 40 inserted between the test signal input terminal 39 and said feedback loop 35a, and the logic of the control signal input terminal 41 is answered, and turning on and off of the 1st and 2nd switch elements 38 and 40 is performed complementary.

[0012] According to this, according to the control voltage from LPF7, the capacity value of the variable-capacity device 36 changes. While being able to stop an oscillation if the phase of oscillation frequency can be tuned finely and the 1st switch element 38 is further made into an OFF state since the capacity value of the capacity 33 of the feedback loop 35 is changed indirectly The test signal (TEST) incorporated through the 2nd switch element 40 can be outputted to DEV3 from the phase inversion element 32.

[0013] Therefore, also in this example, the performance test which contains PC4 in the part and DEV3 list of VCO2 can be performed in digital one at least, and communalization with other trials of a digital IC 1 can be attained.

[0014]

[Effect of the Invention] According to this invention, the performance test which contains PC in the part and DEV list of VCO can be performed in digital one at least, and it can be made the thing suitable for the test atmosphere of a digital IC.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the partial conceptual block diagram of the digital IC of one example.

[Drawing 2] It is the conceptual block diagram of VCO of one example.

[Drawing 3] It is the block diagram of the delay circuit of one example.

[Drawing 4] It is the conceptual block diagram of other VCO of one example.

[Drawing 5] It is the basic block diagram of a PLL circuit.

[Description of Notations]

2: VCO (voltage-controlled oscillator)

2c: Feedback loop

2e: The 1st switch element (control means)

2g: Test signal input terminal

2h: The 2nd switch element (control means)

2i: Control signal input terminal

3: DEV (counting-down circuit)

4: PC (phase comparator)

5: PLL circuit

7: LPF (low pass filter)

35a: Feedback loop

38: The 1st switch element (control means)

39: Test signal input terminal

40: The 2nd switch element (control means)

41: Control signal input terminal

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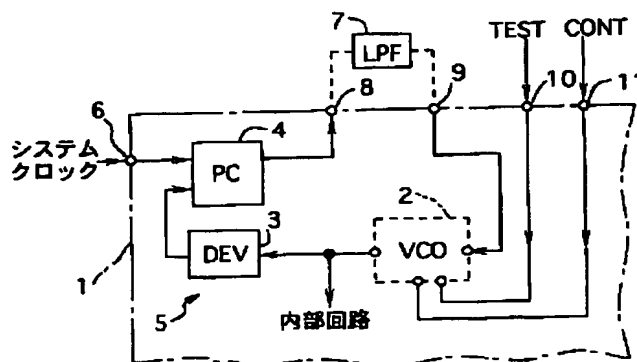
(54) 【発明の名称】 PLL回路

(57) 【要約】

【課題】 デジタル集積回路の試験環境下でPLL回路の試験を行う。

【解決手段】 PLL回路のVCOの帰還路に挿入された第1のスイッチ要素、帰還路とテスト信号入力端子との間に挿入された第2のスイッチ要素、制御信号入力端子の論理に応答して第1及び第2のスイッチ要素のオンオフを相補的に制御する制御手段を備える。第1のスイッチ要素がオフ状態になると、第2のスイッチ要素がオン状態となり、VCOの帰還路が切斷されて発振動作が停止し、第2のスイッチ要素を通して任意のテスト信号がVCOに入力される。したがって、任意のテスト信号をロジックテストで発生するとともに、PCの出力を同テストでモニタすることにより、少なくともVCOの一部とDEV並びにPCを含む動作試験をディジタル的に行える。

一実施例のディジタル集積回路の部分的な概念構成図



- 2: VCO (電圧制御型発振器)
3: DEV (分周器)
4: PC (位相比較器)
5: PLL回路
7: LPF (ローパスフィルタ)

(2)

1

【特許請求の範囲】

【請求項1】制御電圧に応じた周波数の信号を出力する電圧制御型発振器と、該電圧制御型発振器の出力を分周する分周器と、該分周器の出力と基準信号との位相差を検出する位相比較器と、該位相比較器の出力を前記制御電圧に変換するローパスフィルタと、を有するPLL回路において、前記電圧制御型発振器の帰還路に挿入された第1のスイッチ要素と、該帰還路とテスト信号入力端子との間に挿入された第2のスイッチ要素と、制御信号入力端子の論理に

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は、PLL回路に関し、特に、デジタル集積回路に搭載されるPLL回路に関する。

【0002】

【従来の技術】デジタル集積回路の動作速度向上に伴うクロック信号の高周波数化は、一方で機器外部への電波ノイズ放射という問題を少なからず引き起こしているが、PLL(Phase Locked Loop)を用いたクロック信号発生回路は、かかる問題の対策に有効である。

【0003】図5に示すように、PLLは、電圧制御型発振器(VCO)の出力を分周器(DEV)で分周し、その分周出力と基準信号との位相差を位相比較器(PC)で検出し、さらに、その位相差信号をローパスフィルタ(LPF)で直流電圧に変換してVCOの制御電圧とするものであり、VCOやDEVの一部だけが高周波部分となるからである。

【0004】

【発明が解決しようとする課題】しかしながら、かかる従来のPLL回路にあっては、特に、位相比較器(PC)やローパスフィルタ(LPF)の動作がアナログ的であり、デジタル集積回路の試験環境に馴染まないという問題点があった。そこで、本発明は、デジタル集積回路の試験環境でも充分に試験を行えるようにすることとする。

【0005】

【課題を解決するための手段】本発明は、上記目的を達成するために、制御電圧に応じた周波数の信号を出力する電圧制御型発振器(VCO)と、該電圧制御型発振器(VCO)の出力を分周する分周器(DEV)と、該分周器(DEV)の出力と基準信号との位相差を検出する位相比較器(PC)と、該位相比較器(PC)の出力を前記制御電圧に変換するローパスフィルタ(LPF)と、を有するPLL回路において、前記VCOの帰還路に挿入された第1のスイッチ要素と、該帰還路とテスト信号入力端子との間に挿入された第2のスイッチ要素

2

と、制御信号入力端子の論理に応答して前記第1及び第2のスイッチ要素のオンオフを相補的に制御する制御手段と、を備えたことを特徴とする。

【0006】これによれば、第1のスイッチ要素がオフ状態になると、第2のスイッチ要素がオン状態となり、VCOの帰還路が切断されて発振動作が停止するとともに、第2のスイッチ要素を通して任意のテスト信号がVCOに入力される。したがって、任意のテスト信号をロジックテストで発生するとともに、PCの出力を同テストでモニタすることにより、少なくともVCOの一部とDEV並びにPCを含む動作試験をデジタル集積回路の試験環境下で行うことが可能になる。

【0007】

【発明の実施の形態】以下、本発明の実施例を図面に基づいて説明する。図1～図3は本発明に係るPLL回路の一実施例を示す図である。まず、構成を説明する。図1において、1はデジタル集積回路であり、このデジタル集積回路1には電圧制御型発振器2(以下、VCO)、分周器3(以下、DEV)及び位相比較器4(以下、PC)を含むPLL回路5が内蔵されており、このPLL回路5は、端子6に供給されるシステムクロックをn倍(nはDEV3の分周比)した周波数のクロック信号を発生し、内部回路に供給するというものである。なお、PLLの構成要素の一つであるローパスフィルタ7(以下、LPF)は専用の端子8、9に外付けされており、また、10はテスト信号(以下、TEST)を入力するための端子、11は制御信号(以下、CONT)を入力するための端子である。

【0008】VCO2は、図2にその構成を示すように、遅延回路2a及び位相反転素子2b並びに帰還路2cを含む発振部2dと、帰還路2cに挿入された第1のスイッチ要素2eと、遅延回路2aの入力側のノード2fとテスト信号入力端子2gとの間に挿入された第2のスイッチ要素2hと、を有し、第1及び第2のスイッチ要素2e、2hは、制御信号入力端子2iの論理に

応答して相補的にオンオフ(一方がオンすると他方がオフ)するものであり、発明の要旨に記載の制御手段を兼ねるものである。

【0009】遅延回路2aの遅延時間は、LPF7からの制御電圧が所定値のときに、およそ発振周波数の1/2周期(位相差180°)に相当する時間となるように設定されており、位相反転素子2bの位相差と合わせて、発振に必要な360°の位相変化を確保している。因みに、遅延回路2aには、例えば、図3に示す構成のものを使用できる。図3において、端子20と端子21との間に多段に接続された奇数個のインバータ22～26のうちの幾つか(図では22と24の2個)の電源は、定電流源27と可変抵抗要素28を介して供給されており、可変抵抗要素28の抵抗値(nMOSTランジスタ28a～28cのチャネルオン抵抗値)をLPF7

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3

からの制御電圧に応じて増減変化させ、インバータ2、24のしきい値を上下に振ることによって、端子20の論理変化と端子21の論理変化との間に、しきい値変化分に相当する時間差を生じさせるようになっている。

【0010】以上の構成において、デジタル集積回路1をセットしたロジックテスタで、システムクロック、テスト信号(TE ST)及び制御信号(CON T)を発生するとともに、これらの信号をデジタル集積回路1の端子6、端子10及び端子11にそれぞれ印加し、端子8に現れた信号をロジックテスタでモニタすれば、少なくとも、VCO2の一部及びDEV3並びにPC4を含む動作試験をデジタル的に行うことができる。したがって、デジタル集積回路1の他の試験と環境の共通化を図ることができ、試験効率を改善できるという従来技術にない有利な効果が得られる。

【0011】なお、図4はVCOの他の例である。この例は、水晶振動子30と並列に抵抗31、位相反転素子32及び π 型の容量33、34を接続して帰還路35を構成し、さらに、一方の容量33と並列に、LPF7からの制御電圧に応じて容量値を変化させる可変容量デバイス(例えばバリキャップ)36を、直流阻止用の容量37を介して接続するという構成を有するほか、水晶振動子30の一端と位相反転素子32の入力との間の帰還路35aに挿入した第1のスイッチ要素38と、テスト信号入力端子39と前記帰還路35aとの間に挿入した第2のスイッチ要素40とを備え、且つ、第1及び第2のスイッチ要素38、40のオンオフを制御信号入力端子41の論理に応答して相補的に行うというものである。

【0012】これによれば、LPF7からの制御電圧に応じて可変容量デバイス36の容量値が変化し、帰還路35の容量33の容量値を間接的に変化させるから、発振周波数の位相を微調整することができ、さらに、第1のスイッチ要素38をオフ状態にすれば、発振をストッ

4

プできるとともに、第2のスイッチ要素40を介して取り込んだテスト信号(TE ST)を位相反転素子32からDEV3へと出力することができる。

【0013】したがって、この例においても、少なくとも、VCO2の一部及びDEV3並びにPC4を含む動作試験をデジタル的に行うことができ、デジタル集積回路1の他の試験との共通化を図ることができる。

【0014】

【発明の効果】本発明によれば、少なくとも、VCOの一部及びDEV並びにPCを含む動作試験をデジタル的に行うことができ、デジタル集積回路の試験環境に適したものにすることができる。

【図面の簡単な説明】

【図1】一実施例のデジタル集積回路の部分的な概念構成図である。

【図2】一実施例のVCOの概念構成図である。

【図3】一実施例の遅延回路の構成図である。

【図4】一実施例の他のVCOの概念構成図である。

【図5】PLL回路の基本構成図である。

【符号の説明】

2 : VCO (電圧制御型発振器)

2c : 帰還路

2e : 第1のスイッチ要素 (制御手段)

2g : テスト信号入力端子

2h : 第2のスイッチ要素 (制御手段)

2i : 制御信号入力端子

3 : DEV (分周器)

4 : PC (位相比較器)

5 : PLL回路

30 7 : LPF (ローパスフィルタ)

35a : 帰還路

38 : 第1のスイッチ要素 (制御手段)

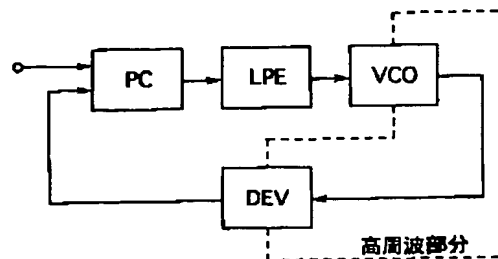
39 : テスト信号入力端子

40 : 第2のスイッチ要素 (制御手段)

41 : 制御信号入力端子

【図5】

PLL回路の基本構成図



【图 1】

- 2: VCO (電圧制御型発振器)
3: DEV (分周器)
4: PC (位相比較器)
5: PLL回路
7: LPF (ローパスフィルタ)

【图 3】

The circuit diagram illustrates a 3-bit digital-to-analog converter (DAC) using a current mirror and a ladder network. The circuit is powered by a VCC supply and grounded. It consists of several key components:

- Input Stage (20):** A differential pair of transistors (20a and 20b) with their sources connected to ground. The gates are connected to a common-mode input signal (20). The drains are connected to VCC and the gates of the first stage of the current mirror (21a and 21b).
- Current Mirror (21):** A three-stage current mirror structure. The first stage (21a, 21b) has its gates connected to the drains of the input stage. The second stage (22a, 22b) has its gates connected to the drains of the first stage. The third stage (23a, 23b) has its gates connected to the drains of the second stage. The sources of all mirror transistors are connected to ground.
- Ladder Network (24):** A network of transistors (24a, 24b, 24c, 24d) and resistors (25a, 25b, 25c) that implements a binary-weighted current summing. The gates of the ladder transistors are connected to the drains of the current mirror stages. The sources of the ladder transistors are connected to ground.
- Output Stage (26):** A differential pair of transistors (26a, 26b) with their sources connected to ground. The gates are connected to the drains of the ladder network. The drains are connected to VCC and the gates of the second stage of the current mirror (22a and 22b).
- Feedback/Reference (27):** A feedback path consisting of a resistor (27a) and a transistor (27b) that connects the output of the ladder network back to the input of the current mirror.
- Low-Pass Filter (LPF):** A block labeled LPF (28) that filters the output signal (28a) to produce the final analog output (28b).

【図 2】

[illegible]

- 2c: 帰還路
2e: 第1のスイッチ要素 (制御手段)
2g: テスト信号入力端子
2h: 第2のスイッチ要素 (制御手段)
2i: 制御信号入力端子

【図 4】

- 35a: 帰還路
38: 第1のスイッチ要素 (制御手段)
39: テスト信号入力端子
40: 第2のスイッチ要素 (制御手段)
41: 制御信号入力端子